WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a data memory which stores data;

a code memory which stores an error checking and correcting code (ECC code) corresponding to the data; and

an error checking and correcting unit (ECC unit) which outputs, to the data memory as the data, a test pattern required to test the data memory, and which generates, from the test pattern, code information having an error checking function, and outputs the code information to the code memory as the error checking and correcting code.

2. The semiconductor device according to claim 1, further comprising:

a test unit which simultaneously tests the data memory and the code memory by reading the test pattern written in the data memory and the code information written in the code memory.

3. The semiconductor device according to claim 2, wherein the ECC unit checks an error on the basis of the code information read from the code memory, and the test unit tests the data memory and the code memory on the basis of results of the error check.

4. The semiconductor device according to claim 1, wherein the ECC unit generates the code information using a Hamming matrix configured so that a sum of row

components of the matrix is odd.

5. The semiconductor device according to claim 2,
wherein the ECC unit generates the code information
using a Hamming matrix configured so that a sum of row
components of the matrix is odd.

6. The semiconductor device according to claim 1,
wherein if all bits of the test pattern are "1"s, the
ECC unit generates the code information so that all
bits of code information generated from the test
pattern are "1"s.

7. The semiconductor device according to claim 2,
wherein if all bits of the test pattern are "1"s, the
ECC unit generates the code information so that all
bits of code information generated from the test
pattern are "1"s.

8. The semiconductor device according to claim 1,
wherein the ECC unit generates the code information so
that all the bits of the code information change from
"0" to "1" or "1" to "0" in accordance with the
inputting of the test pattern.

9. The semiconductor device according to claim 2,
wherein the ECC unit generates the code information so
that all the bits of the code information change from
"0" to "1" or "1" to "0" in accordance with the
inputting of the test pattern.

10. The semiconductor device according to claim 1,
wherein the ECC unit generates the code information so

that an arbitrary N (N is a natural number equal to or

greater than 2) bits of the same address in the test

pattern and in the code information generated from the

test pattern cover all patterns of N-bit combinations

5   in accordance with the inputting of the test pattern.

11.   The semiconductor device according to claim 2,

wherein the ECC unit generates the code information so

that an arbitrary N (N is a natural number equal to or

greater than 2) bits of the same address in the test

10   pattern and in the code information generated from the

test pattern cover all patterns of N-bit combinations

in accordance with the inputting of the test pattern.

12.   The semiconductor device according to claim 1,

wherein the ECC unit generates the code information so

15   that when all the bits of the test pattern other than

one specified bit are "1"s, all the bits of the code

information generated from the test pattern are "1"s.

13.   The semiconductor device according to claim 2,

wherein the ECC unit generates the code information so

20   that when all the bits of the test pattern other than

one specified bit are "1"s, all the bits of the code

information generated from the test pattern are "1"s.

14.   A method of memory test which is applied to a

semiconductor device including a data memory which

25   stores data and a code memory which stores an error

checking and correcting code (ECC code) corresponding

to the data, the method comprising:

generating a test pattern required to test the
data memory;

outputting the test pattern to the data memory;

generating, from the test pattern, code

5   information having an error checking function, and

outputting the code information to the code memory as

the ECC code; and

simultaneously testing the data memory and the

code memory by reading the test pattern written in the

10   data memory and the code information written in the

code memory.

15.   The method according to claim 14, wherein when

the test is executed, it is checked whether or not all

the bits of the code information change from "0" to "1"

15   or "1" to "0".

16.   The method according to claim 14, wherein when

the test is executed, it is checked whether or not an

arbitrary N (N is a natural number equal to or greater

than 2) bits of the same address in the test pattern

20   and in the code information generated from the test

pattern cover all patterns of N-bit combinations in

accordance with the inputting of the test pattern.

17.   The method according to claim 14, wherein when

the test is executed, it is checked whether or not all

25   the bits of the code information generated from the

test pattern are "1"s when all the bits of the test

pattern other than one specified bit are "1"s.